

Features

- Internal control latches and address decoder
- Short set-up and hold times
- Wide operating voltage: 4.5V to 13.2V
- 12Vpp analog signal capability
- R_{ON} 65 Ω max. @ $V_{DD}=12V$, 25°C
- $\Delta R_{ON} \leq 10\Omega$ @ $V_{DD}=12V$, 25°C
- Full CMOS switch for low distortion
- Minimum feedthrough and crosstalk
- Separate analog and digital reference supplies
- Low power consumption ISO-CMOS technology

Applications

- Key systems
- PBX systems
- Mobile radio
- Test equipment /instrumentation
- Analog/digital multiplexers
- Audio/Video switching

Ordering Information

| | |
|---------------------|--------------------|
| MT8808AE | 28 Pin Plastic DIP |
| MT8808AP | 28 Pin PLCC |
| -40° to 85°C | |

Description

The Mitel MT8808 is fabricated in MITEL's ISO-CMOS technology providing low power dissipation and high reliability. The device contains a 8 x 8 array of crosspoint switches along with a 6 to 64 line decoder and latch circuits. Any one of the 64 switches can be addressed by selecting the appropriate six address bits. The selected switch can be turned on or off by applying a logical one or zero to the DATA input. V_{SS} is the ground reference of the digital inputs. The range of the analog signal is from V_{DD} to V_{EE} .

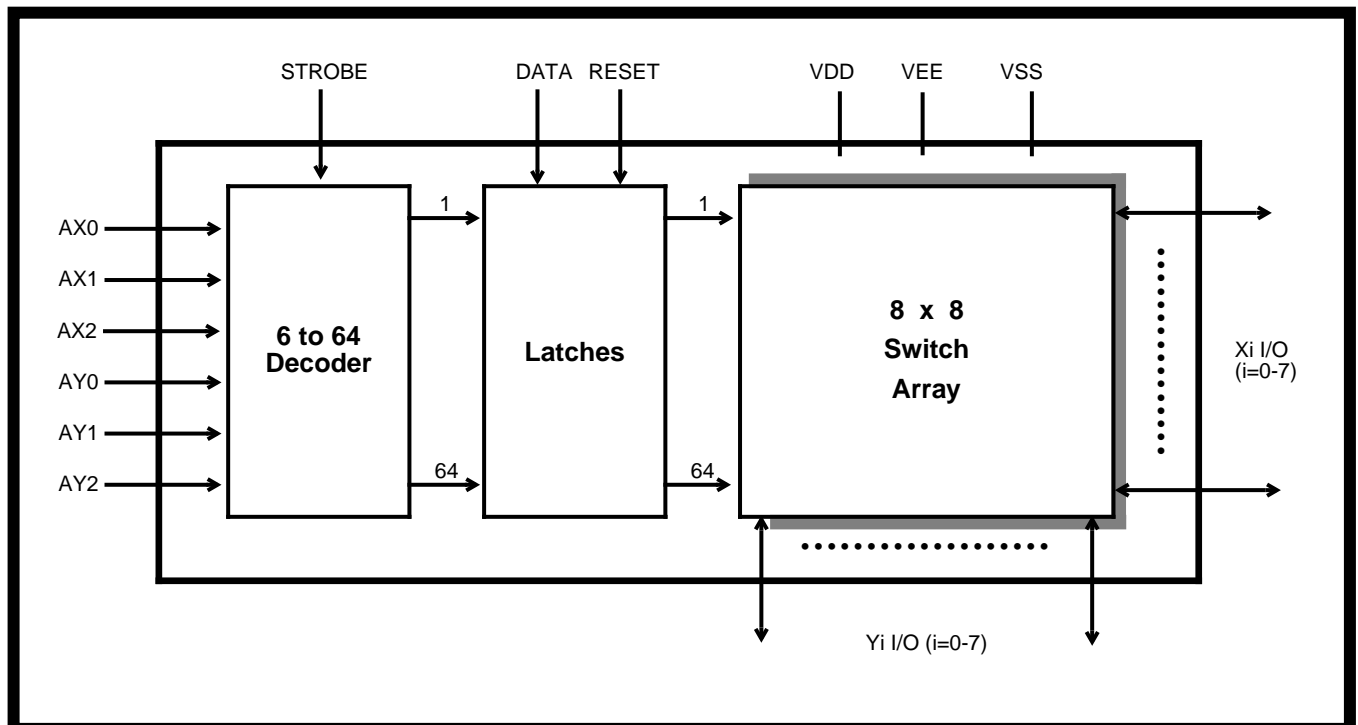


Figure 1 - Functional Block Diagram

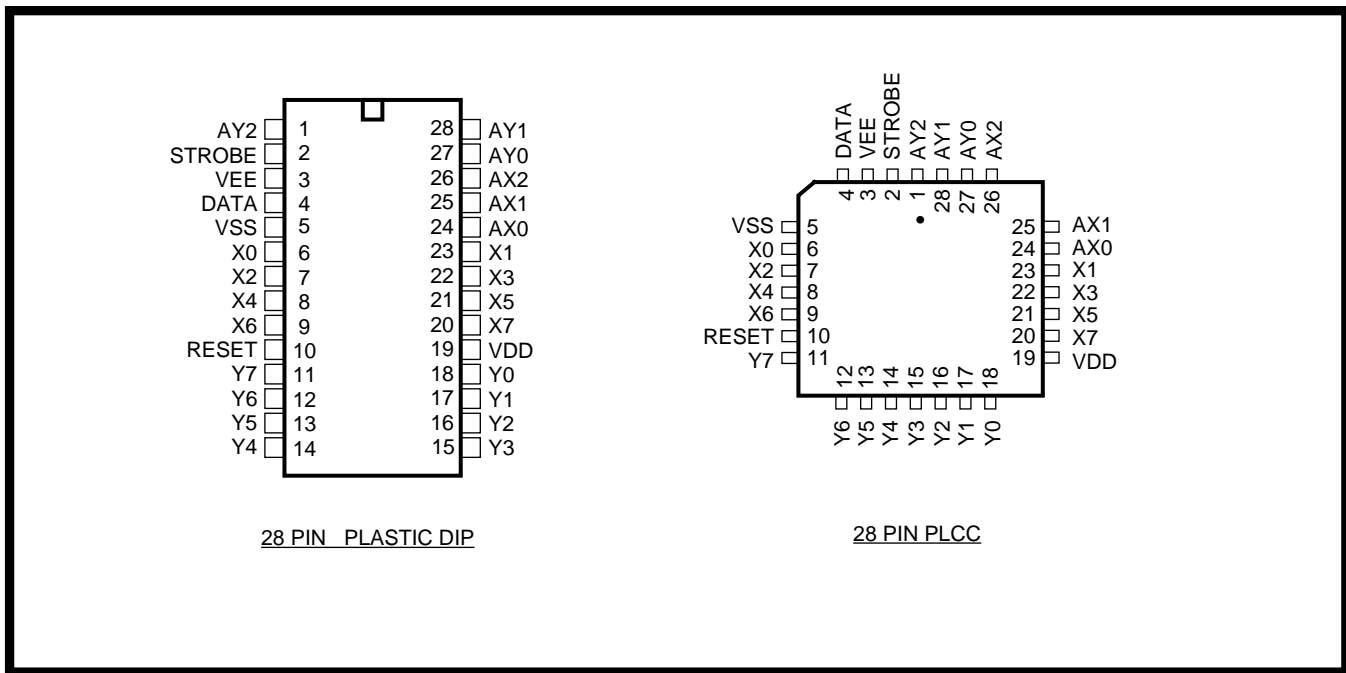


Figure 2 - Pin Connections

Pin Description

| Pin # | Name | Description |
|-------|-----------------|--|
| 1 | AY2 | AY2 Address Line (Input). |
| 2 | STROBE | STROBE (Input): enables function selected by address and data. Address must be stable before STROBE goes high and DATA must be stable on the falling edge of the STROBE. Active High. |
| 3 | V _{EE} | Negative Power Supply. |
| 4 | DATA | DATA (Input): a logic high input will turn on the selected switch and a logic low will turn off the selected switch. Active High. |
| 5 | V _{SS} | Digital Ground Reference . |
| 6-9 | X0, X2, X4, X6 | X0, X2, X4 and X6 Analog (Inputs/Outputs): these are connected to the X0, X2, X4 and X6 rows of the switch array. |
| 10 | RESET | Master RESET (Input): this is used to turn off all switches. Active High. |
| 11-18 | Y7 - Y0 | Y7 - Y0 Analog (Inputs/Outputs): these are connected to the Y0 - Y7 columns of the switch array. |
| 19 | V _{DD} | Positive Power Supply. |
| 20-23 | X7, X5, X3, X1 | X7, X5, X3 and X1 Analog (Inputs/Outputs): these are connected to the X7, X5, X3 and X1 rows of the switch array. |
| 24-26 | AX0-AX2 | AX0 - AX2 Address Lines (Inputs). |
| 27,28 | AY0, AY1 | AY0 and AY1 Address Lines (Inputs). |

Functional Description

The MT8808 is an analog switch matrix with an array size of 8 x 8. The switch array is arranged such that there are 8 columns by 8 rows. The columns are referred to as the Y inputs/outputs and the rows are the X inputs/outputs. The crosspoint analog switch array will interconnect any X I/O with any Y I/O when turned on and provide a high degree of isolation when turned off. The control memory consists of a 64 bit write only RAM in which the bits are selected by the address inputs (AY0-AY2, AX0-AX2). Data is presented to the memory on the DATA input. Data is asynchronously written into memory whenever the STROBE input is high and is latched on the falling edge of STROBE. A logical "1" written into a memory cell turns the corresponding crosspoint switch on and a logical "0" turns the crosspoint off. Only the crosspoint switches corresponding to the addressed memory location are altered when data is written into memory. The remaining switches retain their previous states. Any combination of X and Y inputs/outputs can be interconnected by establishing appropriate patterns in the control memory. A logical "1" on the RESET input will asynchronously return all memory locations to logical "0" turning off all crosspoint switches. Two voltage reference pins (V_{SS} and V_{EE}) are provided for the MT8808 to enable switching of negative analog signals. The range for digital signals is from V_{DD} to V_{SS} while the range for analog signals is from V_{DD} to V_{EE} . V_{SS} and V_{EE} pins can be tied together if a single voltage reference is needed.

Address Decode

The six address inputs along with the STROBE are logically ANDed to form an enable signal for the resettable transparent latches. The DATA input is buffered and is used as the input to all latches. To write to a location, RESET must be low while the address and data are set up. Then the STROBE input is set high and then low causing the data to be latched. The data can be changed while STROBE is high, however, the corresponding switch will turn on and off in accordance with the DATA input. DATA must be stable on the falling edge of STROBE in order for correct data to be written to the latch.

Absolute Maximum Ratings* - Voltages are with respect to V_{EE} unless otherwise stated.

| | Parameter | Symbol | Min | Max | Units |
|---|---------------------------|----------------------|--------------|----------------------|--------|
| 1 | Supply Voltage | V_{DD} V_{SS} | -0.3 -0.3 | 15.0 $V_{DD}+0.3$ | V V |
| 2 | Analog Input Voltage | V_{INA} | -0.3 | $V_{DD}+0.3$ | V |
| 3 | Digital Input Voltage | V_{IN} | $V_{SS}-0.3$ | $V_{DD}+0.3$ | V |
| 4 | Current on any I/O Pin | I | | ±15 | mA |
| 5 | Storage Temperature | T_S | -65 | +150 | °C |
| 6 | Package Power Dissipation | PLASTIC DIP P_D | | 0.6 | W |

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to V_{EE} unless otherwise stated.

| | Characteristics | Sym | Min | Typ | Max | Units | Test Conditions |
|---|-----------------------|----------------------|-----------------|-----|----------------------|--------|-----------------|
| 1 | Operating Temperature | T_O | -40 | 25 | 85 | °C | |
| 2 | Supply Voltage | V_{DD} V_{SS} | 4.5 V_{EE} | | 13.2 $V_{DD}-4.5$ | V V | |
| 3 | Analog Input Voltage | V_{INA} | V_{EE} | | V_{DD} | V | |
| 4 | Digital Input Voltage | V_{IN} | V_{SS} | | V_{DD} | V | |

DC Electrical Characteristics† - Voltages are with respect to $V_{EE}=V_{SS}=0V$, $V_{DD}=12V$ unless otherwise stated.

| | Characteristics | Sym | Min | Typ† | Max | Units | Test Conditions |
|---|---|------------|--------------|------|--------------|---|---|
| 1 | Quiescent Supply Current | I_{DD} | | 1 | 100 | µA | All digital inputs at $V_{IN}=V_{SS}$ or V_{DD} |
| | | | 0.4 | 1.5 | mA | All digital inputs at $V_{IN}=2.4 + V_{SS}$; $V_{SS}=7.0V$ | |
| | | | 5 | 15 | mA | All digital inputs at $V_{IN}=3.4V$ | |
| 2 | Off-state Leakage Current (See G.9 in Appendix) | I_{OFF} | | ±1 | ±500 | nA | $ V_{Xi} - V_{Yj} = V_{DD} - V_{EE}$ See Appendix, Fig. A.1 |
| 3 | Input Logic "0" level | V_{IL} | | | $0.8+V_{SS}$ | V | $V_{SS}=7.5V$; $V_{EE}=0V$ |
| 4 | Input Logic "1" level | V_{IH} | $2.0+V_{SS}$ | | | V | $V_{SS}=6.5V$; $V_{EE}=0V$ |
| 5 | Input Logic "1" level | V_{IH} | 3.3 | | | V | |
| 6 | Input Leakage (digital pins) | I_{LEAK} | | 0.1 | 10 | µA | All digital inputs at $V_{IN} = V_{SS}$ or V_{DD} |

† DC Electrical Characteristics are over recommended temperature range.

‡ Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

DC Electrical Characteristics- Switch Resistance - V_{DC} is the external DC offset applied at the analog I/O pins.

| | Characteristics | Sym | 25°C | | 70°C | | 85°C | | Units | Test Conditions |
|-----|---|-----------------|------|-----|------|-----|------|-----|-------|---|
| | | | Typ | Max | Typ | Max | Typ | Max | | |
| 1 | On-state Resistance $V_{DD}=12V$ $V_{DD}=10V$ $V_{DD}=5V$ (See G.1, G.2, G.3 in Appendix) | R_{ON} | 45 | 65 | | 75 | | 80 | Ω | $V_{SS}=V_{EE}=0V$, $V_{DC}=V_{DD}/2$, $ V_{Xi}-V_{Yj} = 0.4V$ See Appendix, Fig. A.2 |
| 55 | | | 75 | | 85 | | 90 | | | |
| 120 | | | 185 | | 215 | | 225 | | | |
| 2 | Difference in on-state resistance between two switches (See G.4 in Appendix) | ΔR_{ON} | 5 | 10 | | 10 | | 10 | Ω | $V_{DD}=12V$, $V_{SS}=V_{EE}=0$, $V_{DC}=V_{DD}/2$, $ V_{Xi}-V_{Yj} = 0.4V$ See Appendix, Fig. A.2 |

AC Electrical Characteristics[†] - Crosspoint Performance - Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

| | Characteristics | Sym | Min | Typ [‡] | Max | Units | Test Conditions |
|---|--|-------------------|-----|------------------|-----|-------|---|
| 1 | Switch I/O Capacitance | C_S | | 20 | | pF | $f=1$ MHz |
| 2 | Feedthrough Capacitance | C_F | | 0.2 | | pF | $f=1$ MHz |
| 3 | Frequency Response Channel "ON" $20\text{LOG}(V_{OUT}/V_{Xi})=-3\text{dB}$ | $F_{3\text{dB}}$ | | 45 | | MHz | Switch is "ON"; $V_{INA} = 2\text{Vpp}$ sinewave; $R_L = 1\text{k}\Omega$ See Appendix, Fig. A.3 |
| 4 | Total Harmonic Distortion (See G.5, G.6 in Appendix) | THD | | 0.01 | | % | Switch is "ON"; $V_{INA} = 2\text{Vpp}$ sinewave $f= 1\text{kHz}$; $R_L=1\text{k}\Omega$ |
| 5 | Feedthrough Channel "OFF" Feed.= $20\text{LOG}(V_{OUT}/V_{Xi})$ (See G.8 in Appendix) | FDT | | -95 | | dB | All Switches "OFF"; $V_{INA}= 2\text{Vpp}$ sinewave $f= 1\text{kHz}$; $R_L= 1\text{k}\Omega$. See Appendix, Fig. A.4 |
| 6 | Crosstalk between any two channels for switches X_i - Y_i and X_j - Y_j . $X_{\text{talk}}=20\text{LOG}(V_{Yj}/V_{Xi})$. (See G.7 in Appendix). | X_{talk} | | -45 | | dB | $V_{INA}=2\text{Vpp}$ sinewave $f= 10\text{MHz}$; $R_L = 75\Omega$. |
| | | | | -90 | | dB | $V_{INA}=2\text{Vpp}$ sinewave $f= 10\text{kHz}$; $R_L = 600\Omega$. |
| | | | | -85 | | dB | $V_{INA}=2\text{Vpp}$ sinewave $f= 10\text{kHz}$; $R_L = 1\text{k}\Omega$. |
| | | | | -80 | | dB | $V_{INA}=2\text{Vpp}$ sinewave $f= 1\text{kHz}$; $R_L = 10\text{k}\Omega$. Refer to Appendix, Fig. A.5 for test circuit. |
| 7 | Propagation delay through switch | t_{PS} | | | 30 | ns | $R_L=1\text{k}\Omega$; $C_L=50\text{pF}$ |

[†] Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.

[‡] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

Crosstalk measurements are for Plastic DIPS only, crosstalk values for PLCC packages are approximately 5dB better.

AC Electrical Characteristics[†] - Control and I/O Timings - Voltages are with respect to $V_{DD}=5V$, $V_{SS}=0V$, $V_{EE}=-7V$, unless otherwise stated.

| | Characteristics | Sym | Min | Typ [‡] | Max | Units | Test Conditions |
|----|--|--------------------|-----|------------------|-----|-------|---|
| 1 | Control Input crosstalk to switch (for CS, DATA, STROBE, Address) | CX_{talk} | | 30 | | mVpp | $V_{IN}=3V$ squarewave; $R_{IN}=1\text{k}\Omega$, $R_L=10\text{k}\Omega$. See Appendix, Fig. A.6 |
| 2 | Digital Input Capacitance | C_{DI} | | 10 | | pF | $f=1\text{MHz}$ |
| 3 | Switching Frequency | F_O | | | 20 | MHz | |
| 4 | Setup Time DATA to STROBE | t_{DS} | 10 | | | ns | $R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$) |
| 5 | Hold Time DATA to STROBE | t_{DH} | 10 | | | ns | $R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$) |
| 6 | Setup Time Address to STROBE | t_{AS} | 10 | | | ns | $R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$) |
| 7 | Hold Time Address to STROBE | t_{AH} | 10 | | | ns | $R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$) |
| 8 | STROBE Pulse Width | t_{SPW} | 20 | | | ns | $R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$) |
| 9 | RESET Pulse Width | t_{RPW} | 40 | | | ns | $R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$) |
| 10 | STROBE to Switch Status Delay | t_S | | 40 | 100 | ns | $R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$) |
| 11 | DATA to Switch Status Delay | t_D | | 50 | 100 | ns | $R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$) |
| 12 | RESET to Switch Status Delay | t_R | | 35 | 100 | ns | $R_L= 1\text{k}\Omega$, $C_L=50\text{pF}$) |

[†] Timing is over recommended temperature range. See Fig. 3 for control and I/O timing details.

Digital Input rise time (t_r) and fall time (t_f) = 5ns.

[‡] Typical figures are at 25°C and are for design aid only; not guaranteed and not subject to production testing.

) Refer to Appendix, Fig. A.7 for test circuit.

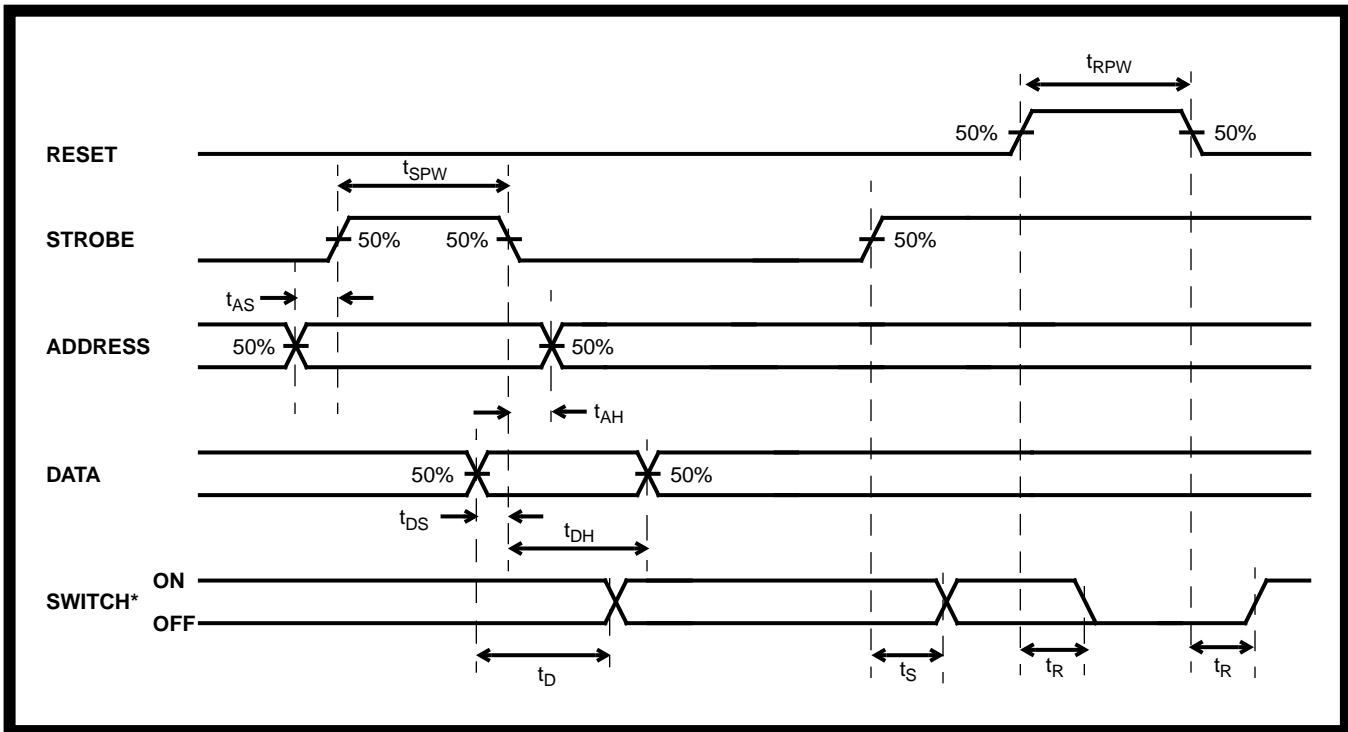


Figure 3 - Control Memory Timing Diagram

* See Appendix, Fig. A.7 for switching waveform

| AY2 | AY1 | AY0 | AX2 | AX1 | AX0 | Connection | AY2 | AY1 | AY0 | AX2 | AX1 | AX0 | Connection |
|-----|-----|-----|-----|-----|-----|------------|-----|-----|-----|-----|-----|-----|------------|
| 0 | 0 | 0 | 0 | 0 | 0 | X0 Y0 | 1 | 0 | 0 | 0 | 0 | 0 | X0 Y4 |
| 0 | 0 | 0 | 0 | 0 | 1 | X1 Y0 | 1 | 0 | 0 | 0 | 0 | 1 | X1 Y4 |
| 0 | 0 | 0 | 0 | 1 | 0 | X2 Y0 | 1 | 0 | 0 | 0 | 1 | 0 | X2 Y4 |
| 0 | 0 | 0 | 0 | 1 | 1 | X3 Y0 | 1 | 0 | 0 | 0 | 1 | 1 | X3 Y4 |
| 0 | 0 | 0 | 1 | 0 | 0 | X4 Y0 | 1 | 0 | 0 | 1 | 0 | 0 | X4 Y4 |
| 0 | 0 | 0 | 1 | 0 | 1 | X5 Y0 | 1 | 0 | 0 | 1 | 0 | 1 | X5 Y4 |
| 0 | 0 | 0 | 1 | 1 | 0 | X6 Y0 | 1 | 0 | 0 | 1 | 1 | 0 | X6 Y4 |
| 0 | 0 | 0 | 1 | 1 | 1 | X7 Y0 | 1 | 0 | 0 | 1 | 1 | 1 | X7 Y4 |
| 0 | 0 | 1 | 0 | 0 | 0 | X0 Y1 | 1 | 0 | 1 | 0 | 0 | 0 | X0 Y5 |
| 0 | 0 | 1 | 0 | 0 | 1 | X1 Y1 | 1 | 0 | 1 | 0 | 0 | 1 | X1 Y5 |
| 0 | 0 | 1 | 0 | 1 | 0 | X2 Y1 | 1 | 0 | 1 | 0 | 1 | 0 | X2 Y5 |
| 0 | 0 | 1 | 0 | 1 | 1 | X3 Y1 | 1 | 0 | 1 | 0 | 1 | 1 | X3 Y5 |
| 0 | 0 | 1 | 1 | 0 | 0 | X4 Y1 | 1 | 0 | 1 | 1 | 0 | 0 | X4 Y5 |
| 0 | 0 | 1 | 1 | 0 | 1 | X5 Y1 | 1 | 0 | 1 | 1 | 0 | 1 | X5 Y5 |
| 0 | 0 | 1 | 1 | 1 | 0 | X6 Y1 | 1 | 0 | 1 | 1 | 1 | 0 | X6 Y5 |
| 0 | 0 | 1 | 1 | 1 | 1 | X7 Y1 | 1 | 0 | 1 | 1 | 1 | 1 | X7 Y5 |
| 0 | 1 | 0 | 0 | 0 | 0 | X0 Y2 | 1 | 1 | 0 | 0 | 0 | 0 | X0 Y6 |
| 0 | 1 | 0 | 0 | 0 | 1 | X1 Y2 | 1 | 1 | 0 | 0 | 0 | 1 | X1 Y6 |
| 0 | 1 | 0 | 0 | 1 | 0 | X2 Y2 | 1 | 1 | 0 | 0 | 1 | 0 | X2 Y6 |
| 0 | 1 | 0 | 0 | 1 | 1 | X3 Y2 | 1 | 1 | 0 | 0 | 1 | 1 | X3 Y6 |
| 0 | 1 | 0 | 1 | 0 | 0 | X4 Y2 | 1 | 1 | 0 | 1 | 0 | 0 | X4 Y6 |
| 0 | 1 | 0 | 1 | 0 | 1 | X5 Y2 | 1 | 1 | 0 | 1 | 0 | 1 | X5 Y6 |
| 0 | 1 | 0 | 1 | 1 | 0 | X6 Y2 | 1 | 1 | 0 | 1 | 1 | 0 | X6 Y6 |
| 0 | 1 | 0 | 1 | 1 | 1 | X7 Y2 | 1 | 1 | 0 | 1 | 1 | 1 | X7 Y6 |
| 0 | 1 | 1 | 0 | 0 | 0 | X0 Y3 | 1 | 1 | 1 | 0 | 0 | 0 | X0 Y7 |
| 0 | 1 | 1 | 0 | 0 | 1 | X1 Y3 | 1 | 1 | 1 | 0 | 0 | 1 | X1 Y7 |
| 0 | 1 | 1 | 0 | 1 | 0 | X2 Y3 | 1 | 1 | 1 | 0 | 1 | 0 | X2 Y7 |
| 0 | 1 | 1 | 0 | 1 | 1 | X3 Y3 | 1 | 1 | 1 | 0 | 1 | 1 | X3 Y7 |
| 0 | 1 | 1 | 1 | 0 | 0 | X4 Y3 | 1 | 1 | 1 | 1 | 0 | 0 | X4 Y7 |
| 0 | 1 | 1 | 1 | 0 | 1 | X5 Y3 | 1 | 1 | 1 | 1 | 0 | 1 | X5 Y7 |
| 0 | 1 | 1 | 1 | 1 | 0 | X6 Y3 | 1 | 1 | 1 | 1 | 1 | 0 | X6 Y7 |
| 0 | 1 | 1 | 1 | 1 | 1 | X7 Y3 | 1 | 1 | 1 | 1 | 1 | 1 | X7 Y7 |

Table 1. Address Decode Truth Table